# Development of $CoSi_2$ Salicide Process

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*Abstract* – **As RIT is continuously scaling CMOS technology to smaller dimension, the Self-Aligned Silicide (Salicide) process needs to be developed. The silicided metalization leads to low-resistivity gates, interconnections and contacts between the metal and silicon substrate. Currently, salicide processes, such as titanium silicide ($TiSi_2$) and cobalt silicide ($CoSi_2$), are widely used in advanced CMOS technologies. However, only $CoSi_2$ salicide process is scalable to deep sub-micron technology, since the resistivity of CoSi2 phase is independent of the dimensions.**

**$CoSi_2$ salicide process using titanium nitride (TiN) as capping film has been developed. Electrical tests were performed: low resistivity of the $CoSi_2$ and negligible leakage current between gate and source/drain were measured. However, the films showed the presence of cobalt oxide, which might have been incorporated during sputtering step.**

## 1. INTRODUCTION

The metal silicides have been a topic of intensive research for more than a decade and have been used extensively in the semiconductor industry. Most of its application is developed for advanced sub-micron CMOS technology to lower sheet resistance (and subsequently RC delay) and to reduce the source/drain parasitic resistance, by forming ohmic contacts in the source/drain regions of MOS transistor, thereby increasing the drive current of the transistors.

The purpose of this work was to develop a self-aligned cobalt silicide process to use for advanced sub-micron CMOS technology in Microelectronic Engineering facility at Rochester Institute of Technology. New applications of $CoSi_2$, such as development of high frequency Schottky Junction Transistors [1] and ultra-fast Metal-Semiconductor-Metal photodetector [2], are also possible.

The lines of polysilicon/gate oxide on silicon substrate were used to simulate the MOS gate and drain/source process. Since, the $CoSi_2$ is independent of line width and doping, it is a reasonable to analyze the self-aligned $CoSi_2$ formation. In figure 1, the pattern of serpentine structure is shown, which were used to measure resistance of $CoSi_2$ on top of poly lines:

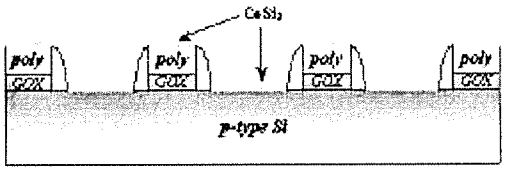



Fig. 1: Cross-section of salicided polysilicon/oxide lines with sidewall spacers to separate poly lines from Si substrate.

## 2. THEORY

### *A. Cobalt*

The general properties of cobalt (Co) is listed in the table below:

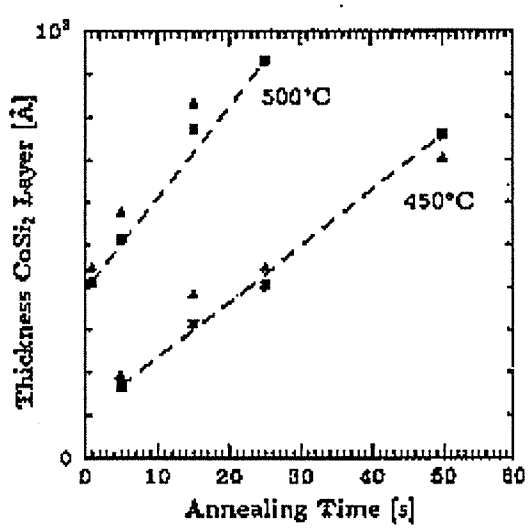
| Property | Value | Conditions |
|---|---|---|
| Atomic Number | 27 | *NA* |
| Atomic Weight | 58.9332 | *NA* |
| Density | 8.9 gm/cc | *NA* |
| Melting Point | 1495 °C | *NA* |
| Boiling Point | 2870 °C | *NA* |
| Thermal Conductivity | 1.00 W/cm/°K | 25 °C |
| Electrical Resistivity | 6.24 μΩ·cm | 20 °C |
| Electronegativity | 1.8 Paulings | *NA* |

Table 1: General material properties of cobalt

### *B. Cobalt Silicide*

Cobalt silicidation involves the conversion of the complete Co film to the cobalt monosilicide (CoSi) phase during a first rapid thermal annealing and a second conversion to the final $CoSi_2$ phase during the second rapid thermal annealing. $CoSi_2$ formation requires an optimal control of the silicidation process and the potential to scale down the process to form thinner layers.

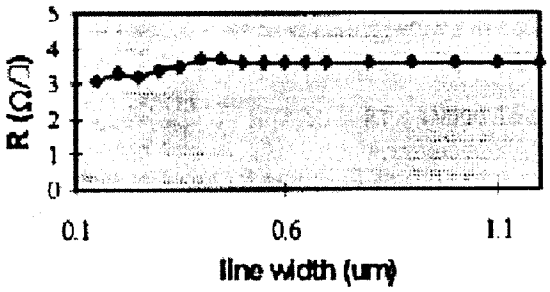
The first anneal of Co plays an important role in the final thickness of the final $CoSi_2$ film. The reaction is diffusion-controlled and results in layer-by-layer growth [3]. The graph 1 shows the thickness of the $CoSi_2$ layers resulting from a limited reaction process as a function of the RTP annealing time for 450 °C and 500 °C:




Graph 1: Thickness of $CoSi_2$ layer vs. anneal time [3]

A selective etch is used to remove the unreacted Co from the $SiO_2$ regions between two silicidation steps to ensure the self-alignment process. The sheet resistance of CoSi is near or even above 40 Ω/?.

The parameters of a second anneal is not critical. It forms $CoSi_2$ by forcing Co to diffuse further into silicon, thus making silicon-rich silicide [4]. The sheet resistance of $CoSi_2$ will not degrade as line width is reduced to sub-quarter micron [5]. This can be seen from the graph below:




Graph 2: $CoSi_2$ sheet resistance vs. line width

## 3. EXPERIMENTAL

To simulate the gate and source/drain structure of CMOS transistor, the gate oxide layer of 20 *nm* was thermally grown on p-type silicon wafers and the polysilicon film of 400 *nm* was deposited, doped with N-250 phosphorous spin-on-glass (SOG) dopant and underwent drive-in step in Bruce Furnace. Next, the SOG dopant was removed by wet etch and polysilicon film was patterned by sub-micron CMOS poly layer mask. After RIE etching patterned polysilicon, the Low Temperature Oxide (LTO) was deposited, densified, and etch-backed to form sidewall spacers. At that point, wafers were ready for sputtering cobalt and titanium nitride films.

### *A. Cobalt Deposition*

Once the CMOS gate structure was simulated, the wafers were ready for sputtering. Patterned and blanket poly wafers were cleaned in $H_2SO_4$:$H_2O_2$ (1:2) solution at 90 °C for 5 minutes to remove any organic and inorganic particles from the surface of the wafers. This was followed by 5-minute rinse and Spin Rinse Dry (SRD). To avoid any native oxide on silicon and polysilicon surfaces, wafers were immersed in hydrofluoric acid (HF) for 20 seconds followed by 5-minute rinse and SRD. This step is critical, since the native oxide is not allowed on the surface where $CoSi_2$ is forming and at the same time the oxide sidewall spacers are present to separate poly lines and silicon substrate. Therefore, the time should be thoroughly controlled for this step.

The wafers were loaded into CVC 601 sputterer and the base pressure of $7.5\times10^{-6}$ *Torr* was achieved. As discussed later, the base pressure needs to be in low $10^{-7}$ or even mid-$10^{-8}$ range to avoid any oxidation of cobalt during sputtering. The condition of sputtering is described in the table below:

| Parameters | Conditions |
|---|---|
| Target Material | Co |
| Target Size | 4" |
| Pre-heat Time | 20 min. |
| Pre-heat Temperature | 300 °C |
| Base Pressure | $7.5\times10^{-6}$ Torr |
| Gas Flow | 58 sccm of Ar |
| Sputter Pressure | $5\times10^{-3}$ Torr |
| Power | 250 Watts |
| Pre-Sputter Time | 5 min. |
| Sputter Time | 5.75 min. |
| Thickness Deposited | ~35 nm |

Table 2: Sputtering conditions for cobalt deposition

It should be noted that pre-heating should be done at the beginning of pump-down to evaporate any water molecules from the substrate. Also, the argon (Ar) gas flow might be different in order to achieve the sputter pressure of 5 *mTorr*.

### *B. Titanium Nitride Deposition*

Titanium nitride (TiN) cap is an important step in $CoSi_2$ formation, since it protects Co from oxidation after the wafers are exposed to atmosphere and during first RTP anneal. It should be done without breaking vacuum. The conditions for TiN sputtering are:

| Parameters | Conditions |
|---|---|
| Target Material | Ti |
| Target Size | 8" |
| Pre-heat Time | same as for Co dep. |
| Pre-heat Temperature | same as for Co dep. |
| Base Pressure | same as for Co dep. |
| Gas Flow 1 | 41 sccm of Ar |
| Gas Flow 2 | 15 sccm of $N_2$ |
| Sputter Pressure | $5\times10^{-3}$ Torr |
| Power | 1000 Watts |
| Pre-Sputter Time | 5 min. |
| Sputter Time | 17 min. |
| Thickness Deposited | ~50 nm |

Table 3: Sputtering conditions for TiN deposition

TiN film of 30-40 *nm* might be sufficient to protect Co from oxidation. Also, TiN cap should be stoichiometric with dark orange color. However, the color of TiN depends on the thickness of the film.

## *C. First RTP Anneal*

The first anneal is performed in AG Associates HeatPulse 410 Rapid Thermal Processor (RTP).

During the first thermal treatment, the deposited Co film is only partially consumed to form an intermediate silicide phase, which is cobalt monosilicide (CoSi). This step is performed at a low temperature. The amount of cobalt consumed for silicidation is completely determined by the temperature and time (see Graph 1). The parameters of first anneal are shown in the table below:

| Parameters | Settings |
|---|---|
| Temperature | 520 °C |
| Time | 20-30 sec. |

Table 4: Settings for first anneal

Even though, the experimental temperature was set at 520 °C, the setting between 450 °C and 500 °C is desirable. However, RTP was not stable below 520 °C. Also, the time needs to be adjusted in order to make the final $CoSi_2$ film thicker. Thirty-second anneal resulted in about 10 *nm* of silicide.

## *D. Removal of Co and TiN*

After the CoSi was formed at polysilicon lines and silicon substrate, the unreacted cobalt and TiN cap must be removed. It was done by wet etching using sulfuric acid-peroxide solution:

| Parameters | Settings |
|---|---|
| $H_2SO_4$:$H_2O_2$ | 1:2 |
| Temperature | 90 °C |
| Time | 1-2 min. |

Table 5: Wet etch parameters and settings

The time might vary to etch off Co and TiN, since the hydrogen peroxide is evaporating, thus changing the proportion of the chemicals. It etches faster for the first wafer. The formed CoSi will not be effected by this etch, so it is not critical if the wafers is overetched.

## *E. Second RTP Anneal*

The second RTP annealing is the final step of the $CoSi_2$ formation. However, it needs to be confirmed that CoSi film has been formed. It can be easily done by measuring sheet resistance using four-point probe. The high sheet resistance of around 40 Ω/? was observed for the wafers after the wet etch. The settings for second anneal are:

| Parameters | Settings |
|---|---|
| Temperature | 750 °C |
| Time | 30-50 sec. |

Table 4: Settings for second anneal

The time was varying from 30-50 seconds, which showed slight improvement in sheet resistance for longer time. It might be due to forming all of CoSi into $CoSi_2$. The sheet resistance went down from 40 Ω/? of CoSi to 17 Ω/?.

# 4. DISCUSSION

## *A. XRD Analysis*

X-Ray Diffraction (XRD) analysis is a certain way to find out the nature of the film. The pattern of a scanned sample of the wafer was compared with the sample of $CoSi_2$ XRD pattern, which was obtained from Alpha Products. It was noticed that all phase peaks were shifted by one degree from the Alpha Products' pattern. Also, one peak of $CoSi_2$ was replaced by the cobalt oxide peak, which might have been caused by oxygen incorporation during the sputtering.

The peak shift was probably resulted from the cobalt oxide peak, which slightly changed the structure of the film. XRD pattern in Figure 2 shows the $CoSi_2$ peak 1 through 4 and peak 5 is cobalt oxide peak. The XRD pattern of $CoSi_2$ (Figure 3) was obtained from Alpha Products.

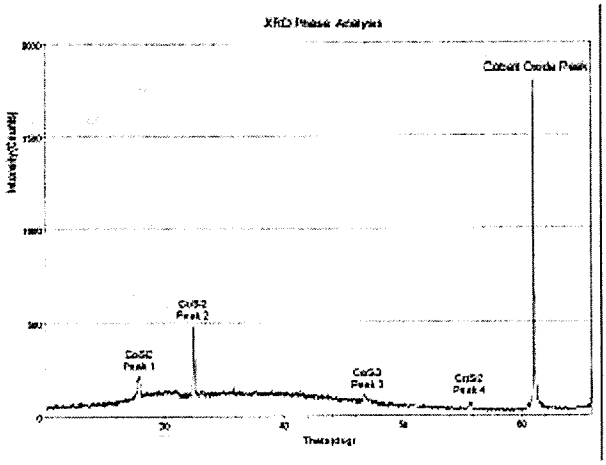


Fig. 2: XRD pattern of $CoSi_2$ from one of the wafers.

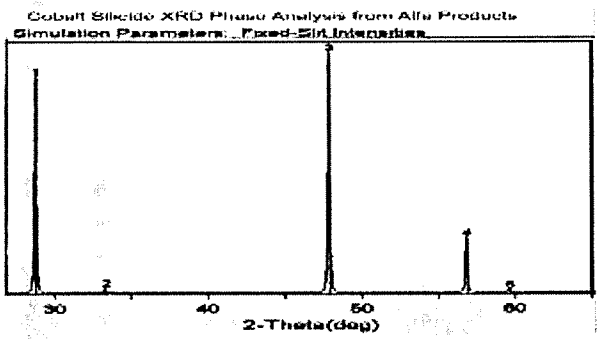



Fig. 3: XRD pattern of $CoSi_2$ from Alpha Products

As it can be seen from figure 2, the cobalt oxide peak at 61 ° is present. Since CVC 601 sputterer does not allow the base pressure go below mid range of $10^{-6}$ Torr, the oxygen molecules are present in the chamber during Co sputtering. This causes oxidation of cobalt, which is very sensitive to oxygen.

## *B. SEM Images*

In order to visually see the cross-section of the structure, the Scanning Electron Microscope (SEM) was used. The figure 4 shows the exact structure of the formed line. The sidewall spacers are formed around poly line. The poly line is about 300 *nm* wide, which is result of isotropic etch in GEC Cell using $SF_6$ gas, since the patterned lines should be around one micron. Also, from the step height at the bottom of poly line, it can be seen that wafer has been overetched during back-etching of sidewall spacers and dipped into HF solution right before the sputtering step. HF solution etched oxide spacers laterally resulting in step height. Cobalt silicide could be seen on silicon substrate. $CoSi_2$ conformed a thin film to silicon substrate surface. However, it is harder to see the $CoSi_2$ on poly line, since the film is very thin (around 10 *nm*). The grains on the substrate are from the CMP slurry, which were deposited during polishing the sample before taking SEM image.

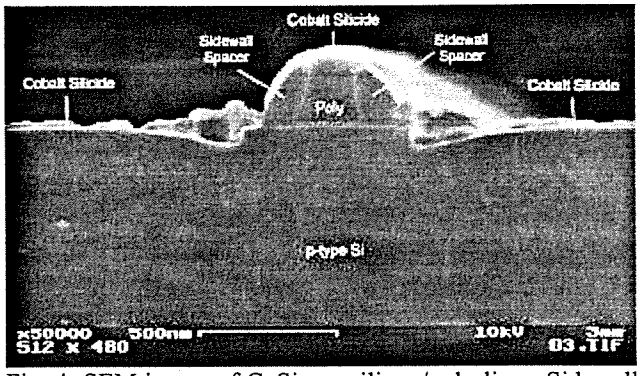



Fig. 4: SEM image of $CoSi_2$ on silicon/poly line. Sidewall spacers prevented $CoSi_2$ formation during annealing.

Here is another SEM image taken from the top angle. It shows that poly lines were overetched.

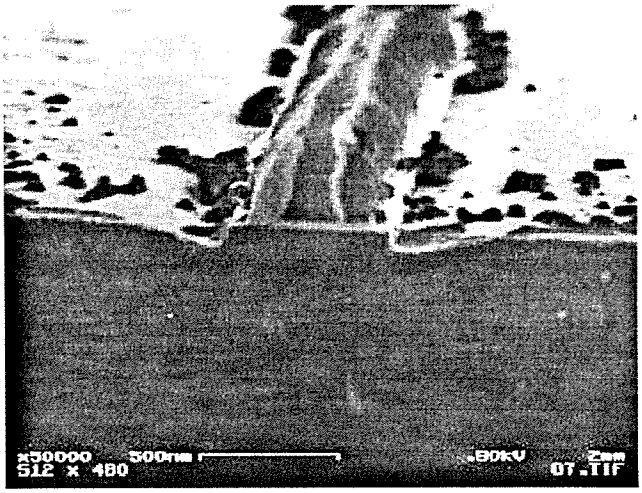



Fig. 5: SEM image of another poly line.

Next image shows the three-micron poly line. The same pattern of sidewall spacers and overetched substrate is observed. It is still hard to see $CoSi_2$ on the line but it is obvious that the film is conformal.

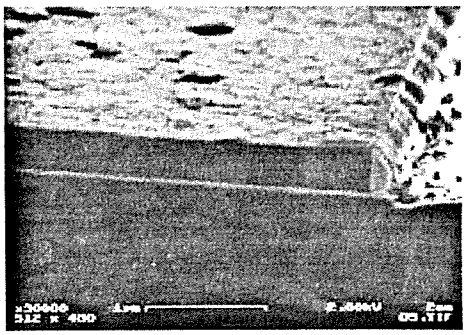


Fig. 5: SEM image of $CoSi_2$ on three-micron poly line.

### *C. Electrical Test*

The tests were performed on HP 4145A Semiconductor Parameter Analyzer to measure the line resistivity and leakage current. The test structures are shown below:

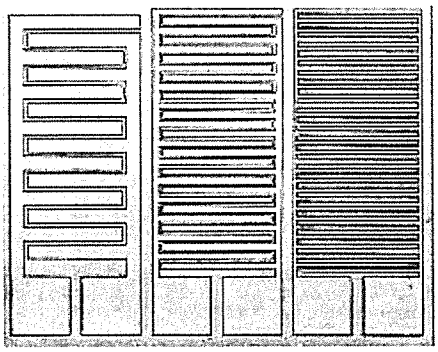


Fig. 6: Comb structures with space separation of 6 μm, 4 μm, and 2 μm (from left to right)

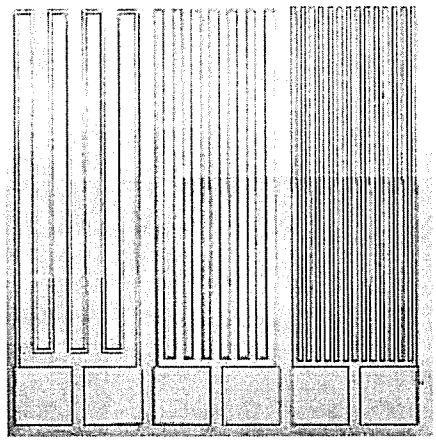


Fig. 7: Serpentine structures with total squares of 890, 2800, and 32000 (from left to right)

The resistance of the comb structures was tested before and after $CoSi_2$ formation. The resistance of the comb space separation prior to $CoSi_2$ layer has been measured on multimeter and showed an infinite resistance, which is greater than 20 MΩ. After the formation of $CoSi_2$, the resistance is shown below:

| Separation | V (V) | I (nA) | R (MΩ) |
|---|---|---|---|
| Small (2 μm) | 2 | 36.7 | 54.5 |
| Medium (4 μm) | 2 | 9.22 | 217 |
| Large (6 μm) | 2 | 3.15 | 635 |

Table 5: Leakage current and resistance between the poly lines of comb structure at 2 V.

The actual separation is not know, however the poly lines underwent an isotropic etched in GEC Cell and got reduced laterally. The resistance and the leakage current are shown to be reasonable if the area of the lines is taken into consideration.

The resistance of serpentine lines was also measured before and after the formation of $CoSi_2$. The resistance and sheet resistance are shown in Table 6:

| Linewidth / Sq. | Before | | After | |
|---|---|---|---|---|
| | R (kΩ) | Rs (Ω/?) | R (kΩ) | Rs (Ω/?) |
| Small / 35000 | 950 | 27.1 | 848 | 24.5 |
| Medium / 2800 | 82.2 | 29.4 | 15.9 | 5.68 |
| Large / 890 | 25.8 | 29.0 | 4.96 | 5.57 |

Table 6: Resistance and sheet resistance of $CoSi_2$/poly serpentine lines before and after $CoSi_2$ formation.

The resistance and sheet resistance of small serpentine line are higher than expected. Since isotropic etch of poly lines in GEC Cell distorted the profile of the line, it is not uniform in width and some areas are thinner than others. It also can be seen on SEM image in figure 5.

## 5. CONCLUSION

Overall, the $CoSi_2$ salicide process has been demonstrated to be successful. It significantly reduced the resistance of the poly lines and silicon substrate surfaces. Also, it has been proven that the self-aligned process is established with negligible leak current and high resistance between the lines and substrate. XRD analysis confirmed the pattern of $CoSi_2$ film.

However, the time for first anneal needs to be increased to make $CoSi_2$ film thicker. Also, if RTP is capable, the temperature needs to be decreased to 450-500 °C for the first anneal step. This will ensure the proper formation of cobalt monosilicide.

Another issue that should be taken into consideration is the cobalt oxide in the $CoSi_2$ film. The base pressure in the sputter tool needs to be in the low $10^{-7}$ or even in the mid-$10^{-8}$ Torr range. This will prevent the oxidation of Co during sputtering.

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